An 8x8 Pixel IC for X-ray Spectroscopy

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Abstract-- **An integrated circuit providing 64 channels of low-noise signal processing electronics in an 8x8 pixel arrangement has been developed as part of an integrated silicon detector array for high count-rate x-ray spectroscopy applications. Each pixel features low-noise charge integration, programmable peaking time and gain, and an output driver. The 8x8 pixel IC builds upon our previous development of the XPS chip, a 1-dimensional preamplifier-shaper IC for linear silicon detector arrays. The new pixel design features significant improvements to the shaper and output driver stages, including digital peaking time and gain selection, and a low-power charge driver/receiver design. When operated with a cooled, low-capacitance silicon detector, an energy resolution of ~210 eV FWHM was obtained for 5.89 keV x rays.**

I. INTRODUCTION

CMOS integrated circuits that provide many channels of low-noise charge-sensitive preamplifiers and signal processing electronics on a single chip have been developed for use with segmented silicon detector arrays. This approach offers the following advantages over discrete designs: a) better noise performance due to reduced detector capacitance and reduced leakage current, b) high total count rate capability by distributing the flux over many channels, c) the availability of position information, and d) relatively low power consumption and mass. Integrating both preamplifier and spectroscopic amplifier features such as variable pulse shaping and programmable gain into a single ASIC can therefore provide a compact, relatively low cost detector system with excellent noise performance.

We have pursued the development of such ASICs for use in x ray fluorescence and x ray absorption spectroscopy detector systems at synchrotron light sources, and for potential use in satellite borne radiation detectors, which require good noise performance, low power consumption, and low weight. For the readout of 1-dimensional silicon diode arrays, the 32 channel XPS IC has previously been developed, and is described in [1]. Each of the 32 parallel channels consists of a charge integrator, variable peaking-time pulse shaper, programmable gain stage, and output driver stage. The performance of the final IC, in the full 64 channel spectroscopy system originally reported on in [2], is described in Section II.

Based on the XPS design, an 8x8 pixel array IC providing 64 channels of low-noise signal processing electronics has been designed as part of an integrated 8x8 silicon detector array for high count-rate, low-noise x-ray applications. The pixel IC will be bump bonded to a pixilated silicon diode array having 1 mm^2 elements. The 2-D layout results in a more compact geometry better suited for most applications, and eliminates the stray capacitance of wire bond connections.

In recent years, other groups have developed CMOS ASICs for silicon and CZT detector arrays that integrate both similar and more complex features, such as pole-zero cancellation and baseline holding circuits [3-6]. Our approach has been straightforward, using a gated feedback scheme and focusing on integrating a large number of channels with relatively low power consumption.

II. A 64 CHANNEL DETECTOR USING THE XPS IC

A 64-channel detector has been constructed using two 32-channel XPS ICs and a single 4x16 element silicon photodiode array. Some features of the XPS operation are reviewed in Section II.A, while measurements performed with the complete detector system are described in Section II.B.

A. Operation of the XPS IC

Each of the 32 channels of the XPS IC collect and process x ray photons independently as described in [1]. Charge from photons absorbed in the detector is integrated onto a 10 fF feedback capacitance in the preamplifier of each channel. The output of the preamplifier is processed by a CR-RC^2 pulse shaper that has a variable peaking time range of 0.5μs-4μs, and programmable gain range of 1 to 8. This processing stage is followed by a programmable gain of 4, and a fixed gain of 10. The output signal is a shaped pulse that ranges approximately 0 to -2 volts, matching the input range of the discrete peak-detecting ADCs designed for the detector system [7]. The output is able to drive a 100pF load in parallel with 10kΩ, which is approximately that of the ADC and 2 meters of ribbon cable.

The preamplifiers are operated in switched-reset mode. A schematic diagram of the reset scheme is given in Figure 1,

and is described as follows: while each channel has its own signal processing chain, there is also a wired-OR output from all 32 preamplifiers that tracks the integrator output voltage for the most active channel. Using this saturation signal as a reference, the reset circuit in each preamplifier is gated "on" at a preset bias level in order to effect the reset. The rate and duration of the reset is controlled by external circuitry, which triggers at a preset value and asserts the reset until the saturation voltage returns to the input reference level. During the time reset is active, the ADCs are gated "off" with an inhibit signal that encloses the entire reset event.
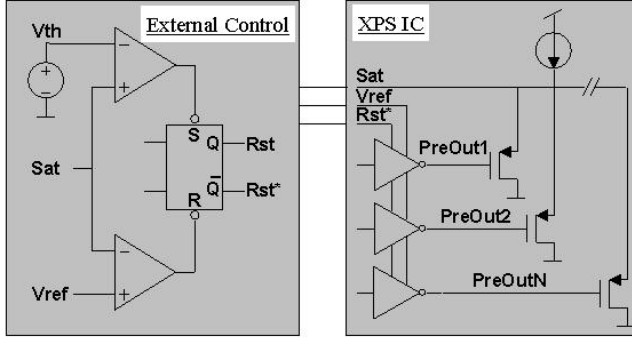

Fig. 1. XPS reset circuit schematic diagram.

An oscilloscope snapshot of the reset circuitry in operation is shown in Figure 2. A large charge injection results from the closing of the reset switch, which results in a large signal transient at the output. The duration of the transient is determined by the settling time of the output stage and its bandwidth setting, which can be adjusted. In the example of Figure 2, the transient lasts ~350μs, which represents a deadtime of ~10% for 5.9 keV photons at a 15 kHz per channel count rate. For modest count rates of a few kHz per channel, the deadtime is <1%.
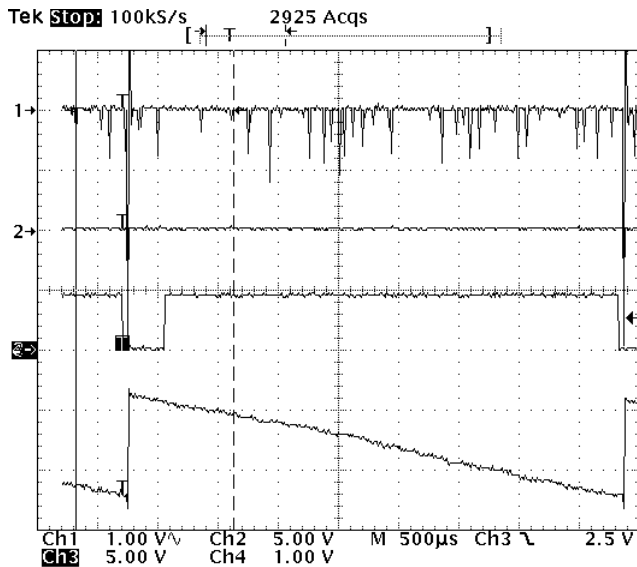
Fig. 2. Oscilloscope snapshot of a reset event. Ch1: Output from a single channel. Ch2: Reset strobe signal (10μs width). Ch3 (third trace): Data acquisition inhibit signal. Ch4 (fourth trace): Saturation indication signal.
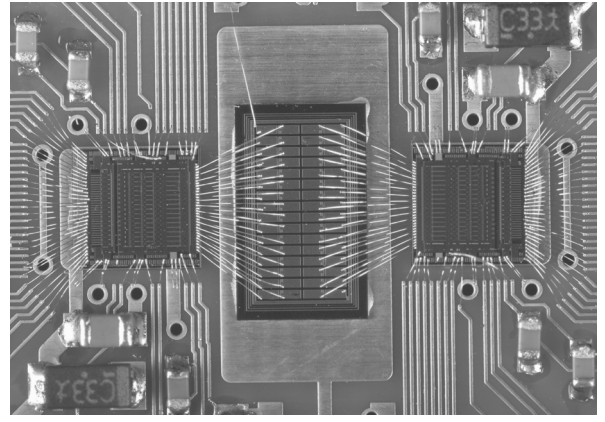
Fig. 3. Detector module photo.

B. Measurements

A prototype detector module is shown in Figure 3. It consists of two 32 channel XPS ICs and a 64 element silicon diode array with capacitance of ~0.2 pF/element. The detector module is housed in a cryostat assembly, which provides thermoelectric cooling, a vacuum chamber, and electrical I/O connections. The entire system consists of a rack-mounted bias and reset control unit, the cryostat containing the detector module, a CAMAC crate with ADC and histogramming memory modules, and a PC [2].

Figure 4: Spectra of the sum of 64 channels. In the first figure (a), the rate is 100 cts/s/channel at 3μs peaking time, the second spectrum, (b), was taken at a rate of 10,000 cts/s/channel at peaking time of 1μs.

[55]Fe spectra measured with the above 64 channel system are shown in Figure 4. The performance of the system at both low and high count rates is shown. Figure 4a represents the the best attainable energy resolution (180 eV FWHM), which was achieved with a low count rate of 100 counts/s/pixel at the optimal peaking time of 3 μs. At higher rates, a shorter peaking time is required to minimize the effects of pileup. The shorter peaking time, however, results in higher thermal noise, decreasing the resolution of the system. The spectrum shown in Figure 4b was taken at a count rate of 10,000 counts/s/pixel corresponding to a total count rate of 640,000 counts/s. In this case, an energy resolution of 240 eV FWHM was measured at a peaking time of 1 μs.

III. THE 8X8 PIXEL IC

The previous work on the XPS IC has led to the development of an 8x8 pixel detector assembly for high-rate, low-noise x-ray spectroscopy. Two versions of the IC have been fabricated and tested: a 2x2 prototype, and a full 8x8 array. In Section III.A, design work is discussed. In Section III.B, some initial test results are given.

A. IC Design
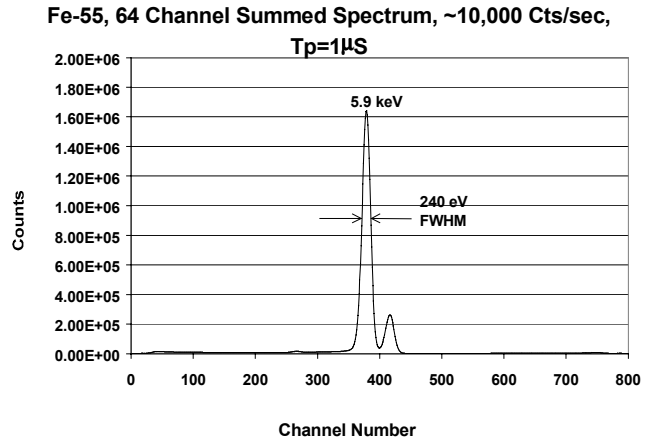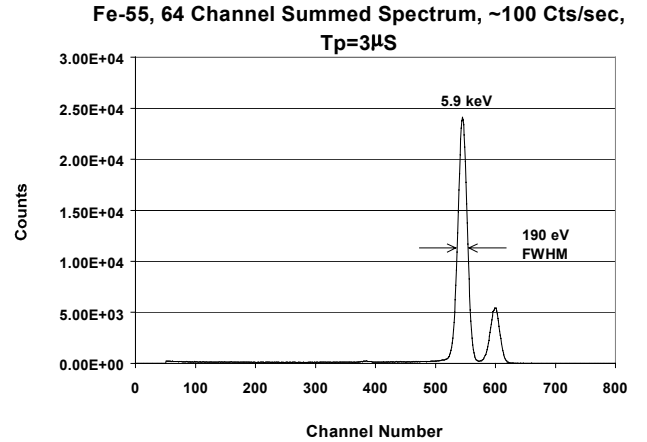
Several improvements were implemented on the 8x8 IC as follows: 1) a 4-bit, digitally programmable peaking time range of 0.5μs to 7.5μs, replacing continuously variable analog controls as proposed in [2], 2) a CR-RC[4] shaper for better noise performance and narrower pulse shape, 3) modified charge integrator designed for 3.3V operation, 4) a new "active termination" output stage design which places the burden of driving the interface cable on the discrete charge receiver, and 5) digital settings for channel disable, calibration, gain and peaking time are stored in an on-chip shift register. A block diagram of this new scheme is shown in Figure 5.

Modifications to the switched-reset XPS charge integrator include a single transistor reset feedback with replica bias, such as that used in [3], and removal of the input transistor's active cascode load, which was necessary in order to provide the required linear output range of 45,000 electrons (five maximum energy pulses of 9000 electrons) with the reduced 3.3V supply. A calibration input and a channel disable feature are also provided. The channel disable is accomplished by switching the shaper input to a DC reference voltage (Vout) just after the capacitor network. This feature is used to disable all channels (Gdis) during a reset event, thereby preventing a large output transient on all channels

The new shaper section uses a 4-bit binary capacitor array with fixed-current, high-linearity transconductors, rather than the fixed capacitance variable transconductance XPS design. The new design allows the peaking time to be easily and accurately programmed once a single bias voltage (Vshap) has been calibrated for the correct peaking time range. A non-inverting gain block is provided following each RC stage to normalize the input signal to a maximum value for each successive stage, thereby minimizing degradation of the signal-to-noise ratio of the processed signal.

It is necessary to consider the noise contribution of the filters in this case, because the impedances of the elements used are necessarily large due to power and space limitations. In this design, tradeoffs exist between the transconductance and the capacitance required to achieve a given time constant. Larger values of tranconductance minimize the noise contribution of the filter, but require larger capacitance values, which in turn require more power to drive, especially at the integrator output where the values are 6 times larger in order to achieve a gain of 6 in the first shaping filter. Larger capacitors, i.e. >10's of pF, also occupy a relatively large area even when a high-value capacitor option is provided by the fabrication process. In this design, a transconductance of ~4 microsiemens results in a minimal noise contribution for the five filter stages, which is diminished in each succeeding filter by the integral gain stages. The corresponding maximum capacitance for the largest time constant in this design is

Fig. 5. Pixel cell schematic diagram

~7.5pF. As is the case for the XPS shaper, high-linearity transconductor designs are required in order to maintain signal integrity over a wide input signal range [8].

A 5-bit programmable gain stage is AC-coupled to the shaper output, and also acts as the output stage. A block diagram of the output stage and its discrete receiver is shown in Figure 6. The "active termination" design uses a small series capacitor at the output of the gain stage to couple it to the pad. The rest of the circuit is formed by a single-ended cable and a standard charge-sensitive amplifier. The voltage output of this stage is the ratio of the feedback capacitance to the on-chip coupling capacitance. Since the external connection point is a virtual ground node, the output stage sees only the series capacitance load (1pF) so that the cable capacitance is irrelevant, which removes the necessity for a large on-chip driver. These conditions hold true so long as the loop gain of the charge receiver is high. A gain-stage bandwidth control is provided (Vbw) to adjust the low-frequency cutoff of the AC-coupling so that the pulse shape will not be distorted.
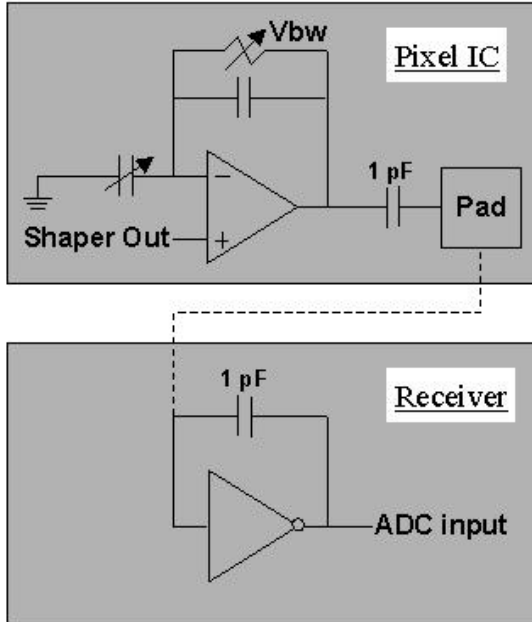
Fig. 6. "Active termination" output stage.

During the simulation phase of the overall design, a resistor network representing all of the significant interconnect busses was generated for the pixel cell, and for the vertical and horizontal power and bias busses. This circuit was used as a module into which the extracted layout was inserted, thereby modeling both the capacitive and resistive elements of the top-level design. Using this model, assessment of the power supply partitioning and power distribution busses resulted in significant improvements in the simulated performance, allowing the response of pixels at extreme geographic locations on the die to be compared. This is of particular importance for self-triggered, asynchronous channels

operating simultaneously, as it is necessary to minimize the transient effects of one channel on another.

B. Measurements

The 8x8 array has been fabricated in 0.5μm CMOS, occupying an area of approximately $1cm^2$. The layout pitch of the IC was dictated by the detector geometry, which resulted in dense pockets of integrated devices in a relatively sparse overall layout. A relatively generous area has thereby been provided for power distribution and bias busses, which is a great benefit for larger devices.
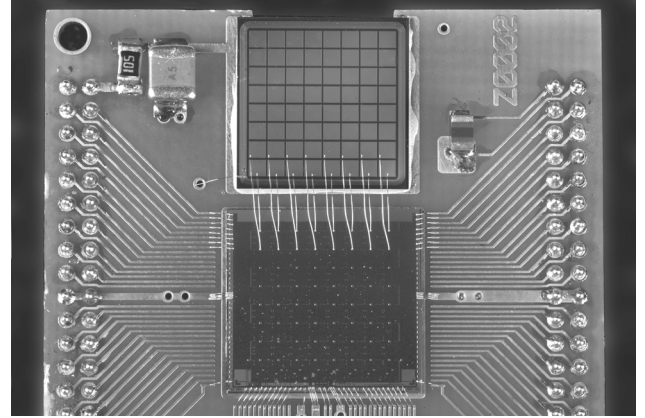

Fig. 7. 8x8 array IC wire-bonded to pixel detector.

A photo of the 8x8 ASIC, wire-bonded to a silicon detector array is shown in Figure 7. The diode array consists of 64 pixels with a $1mm^2$ area each. The capacitance per pixel is ~0.3pF. The wire-bond arrangement has been used for initial tests, whereas the final hybrid assembly will consist of the pictured detector bump-bonded to the ASIC. Basic testing of both the 8x8 array and a prototype 2x2 array have shown that the salient features of the design, i.e. the preamplifier, shaper, gain, and bias and control stages, have been implemented successfully.
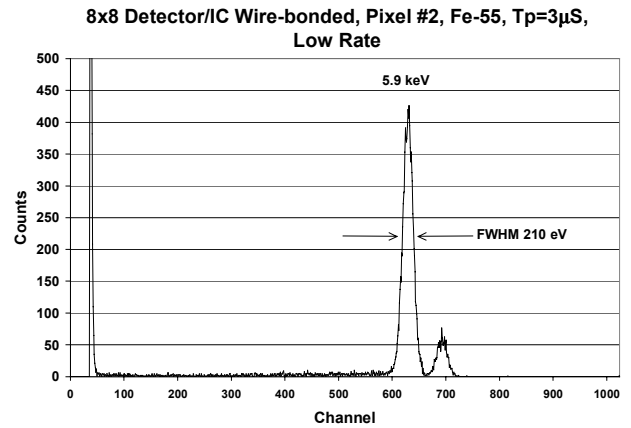

Fig. 8. A single channel 55Fe spectra collected at low rate with the 8x8 array IC wire-bonded to a pixel detector.

The channel-to-channel isolation of adjacent outputs was of particular concern in this design since the relatively large die size requires long, parallel output traces. For this reason, the

output coupling capacitor was placed at the pixel, which effectively treats the long metallization as part of the virtual ground node. An oscilloscope measurement of the response of two adjacent channels connected to the receiver with a 1 meter coax cable indicates that the adjacent channel coupling is approximately +/-1%.

X-ray spectra were acquired with a pixilated silicon detector wire-bonded to the 8x8 array using a ^{55}Fe source. The noise performance of this arrangement is ~210eV FWHM with the (~ -10C) cooled assembly. A single-channel spectrum is shown in Figure 8.

IV. CONCLUSION

Multi-channel CMOS ASICs designed for low-noise x-ray spectroscopy applications have been designed and fabricated in both linear (1-D) and pixel (2-D) format. The performance of the 32 channel linear array XPS IC has been demonstrated in test measurements with a 64-channel system, achieving an energy resolution of < 200eV FWHM for 5.89keV x rays. An 8x8 pixel array IC based on the XPS design has been designed and tested. The IC will be bump-bonded to pixilated silicon diode arrays. Improvements over the XPS IC include convenient use of shift registers for digital programming of most functions, CR-RC^4 pulse shaping, and a low power ouput stage design. Due to careful layout the channel-to-channel coupling has been kept at <1% for adjacent channels. In initial tests of the ICs wire-bonded to pixilated detectors an energy resolution of ~210eV FWHM has been measured for the 5.89keV x rays. The integration of preamplifier and spectroscopic amplifier, with features such as variable pulse shaping and programmable gain, into a multi-channel ASIC provides a compact, relatively low cost detector readout with excellent noise performance. Such ASICs are suitable for use in x ray fluorescence and x ray absorption spectroscopy, and for radiation detection in satellite missions.

V. ACKNOWLEDGMENT

VI. REFERENCES

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